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On-Chip Capacitor

See 1st Attached Sheet

Background and Summary of the Invention

The present invention relates to integrated circuit structures, and particularly to on-chip capacitors.

Background

In integrated circuit fabrication, many devices are placed on a single substrate. The various devices must be electrically isolated from one another, but some specific devices must be electrically interconnected to implement a desired circuit function. Many circuits require more than one level of interconnect, so multi-level interconnect structures are used.

One aim of integrated circuit technology is an increase in device speed. This objective has caused integrated circuit fabrication to seek ways of scaling down devices, increasing the functional complexity of the integrated circuit as a whole. However, downscaling of ICs, and therefore speed, is limited by interconnect technology. One problem with multi-level interconnect structures is the filling of high aspect ratio and varying depth contact holes and vias. Many processes have been developed to address these issues. Another problem is the tendency of closely situated conductors to crosstalk, where potential change in one line affects performance of a nearby line.

The damascene process is one method of forming metallized patterns on ICs. First a conductor pattern is etched into a dielectric layer to form grooves within the dielectric layer. A metal is then deposited to fill the etched grooves. Often an interim step is included

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This application is a continuation of serial number 09/935,519 filed 08/23/2001 now patent number 6,635,916, which claims benefit of serial number 60/229,488 filed 08/31/2000.